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APPLICATION NO. FIRST NAMED INVENTOR ATTORNEY DOCKET NO. FILING DATE CONFIRMATION NO. 08/18/2003 10/642,856 Martin Freitag

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EXAMINER

GRAHAM, KRETELIA

ART UNIT

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)	
		10/642,856	FREITAG ET AL.	
	Office Action Summary	Examiner	Art Unit	
		Kretelia Graham	2827	
The MAILING DATE of this communication appears on the cover sheet with the correspondence address				
Period for Reply				
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).				
Status				
1)⊠	Responsive to communication(s) filed on 19 Se	eptember 2006.		
2a)⊠	This action is FINAL . 2b) This	action is non-final.		
3)				
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.				
Disposition of Claims				
4) 🖂	Claim(s) 1,2 and 4-7 is/are pending in the appli	cation.		
	4a) Of the above claim(s) is/are withdrawn from consideration.			
5) Claim(s) is/are allowed.				
6)⊠	6)⊠ Claim(s) <u>1 and 4</u> is/are rejected.			
7)⊠ Claim(s) <u>2 and 5-7</u> is/are objected to				
8) Claim(s) are subject to restriction and/or election requirement.				
Application Papers				
9) The specification is objected to by the Examiner.				
10)⊠ The drawing(s) filed on <u>18 August 2003</u> is/are: a)⊠ accepted or b)⊡ objected to by the Examiner.				
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).				
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).				
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.				
Priority under 35 U.S.C. § 119				
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).				
a)⊠ All b)□ Some * c)□ None of:				
 Certified copies of the priority documents have been received. 				
2. Certified copies of the priority documents have been received in Application No.				
	3. Copies of the certified copies of the prior	•	ed in this National Stage	
* ~	application from the International Bureau		4	
* See the attached detailed Office action for a list of the certified copies not received.				
Attachment(s)				
	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948)	4) Linterview Summary Paper No(s)/Mail Da	(PTO-413) ate	
3) Anform	mation Disclosure Statement(s) (PTO/SB/08) or No(s)/Mail Date 7/31/06.	5) Notice of Informal P 6) Other:		

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DETAILED ACTION

Response to Arguments

- 1. Applicant's arguments filed 9/19/2006, with respect to the objections to the drawings and specification and rejection of the claims under 35 USC 112 second paragraph have been fully considered and are persuasive. The objections to the drawings and specification and rejection of the claims under 35 USC 112 have been withdrawn.
- 2. Applicant's arguments filed 9/19/2006 have been fully considered but they are not persuasive. Contrary to the applicant's arguments, the US patent to Nakao (6,509,621 B2), hereafter "Nakao" does in fact disclose the steps and device for writing to a MRAM memory device as outlined in amended claims 1 and 4. The relevance of Nakao to the present application is discussed below in the rejection of the claims under 35 USC 102(e).

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

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Claim Objections

4. Claims 1 and 4 are objected to because of the following informalities:

Pertaining to claim 1, the "word line current" of claim 1, lines 18 and 23 lack proper antecedent basis. The claim limitation "nor cells situated on the selected lines" of claim 1, lines 21-22 is unclear. It is unclear as to which cell are not switched since the "selected lines" lacks proper antecedent basis.

Pertaining to claim 4, the "magnetic field produced by the supposition of the magnetic fields of the word line current and a bit line current" of claim 4, lines 17-19 and "word line current" of claim 4, lines 18 and 24 lack proper antecedent basis. The claim limitation "nor cells situated on the selected lines" of claim 4, lines 22-23 is unclear. It is unclear as to which cell are not switched since the "selected lines" lacks proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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6. Claims 1 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakao.

Pertaining to claim 1, FIG. 3A and FIG. 9A-9B are directed towards: A method for writing to magnetoresistive memory cells of an MRAM memory, the magnetoresistive memory cells having a multilayer system containing layers 1-3 stacked one above another, the layers including a soft-magnetic layer 2, a hard-magnetic layer 1 and a tunnel oxide layer 3 disposed between the soft- magnetic layer and the hard-magnetic layer, which comprises the steps of: impressing write currents IWx, IWy being in each case impressed on a respective word line 4 and a respective bit line 5 resulting in a superposition of magnetic fields generated by the write currents, and in each selected memory cell selected by the respective word line and the respective bit line, a magnetic field Hx. Hy leads to a change of a magnetization direction of only the soft-magnetic layer Note: It is inherent for free layer 2 of FIG. 3A to be the only layer capable of having a variable magnetization direction (see column 5, lines 6-11), the write currents being impressed on the respective word line and the respective bit line causing the magnetic field produced by the superposition of the magnetic fields of the word line current and a bit line current to be precisely large enough to suffice for switching the magnetization of the soft magnetic layer in the selected memory cell but small enough that neither adjacent cells nor cells situated on the selected lines are switched see column 10, lines 32-52; Note: It is inherent that the term "adjacent" disclosed in column 10, lines 32-52 also refers to cells on the same selected line, the timings of the impression of both the word line current and the bit line current being exactly

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controlled so that the conventional switching of the soft magnetic layer of the selected memory cell is transferred into a magnetization rotation process rotating said magnetization direction of the soft magnetic layer in a plurality of successive steps in direction desired for writing a logic "0" or "1" Note: Application of word line current lwx and bit line current lwy are done in a specified time period of 1ns so that the magnetization direction is switched according to FIG. 9A-9E (see column 9, line 46 – column 10, line 12. Additionally, it is inherent to write either a logic "0" or logic "1" to a memory cell.

Pertaining to claim 4, FIG. 3A and 5A of Nakao are directed towards: an array 30 containing magnetoresistive memory cells 27 each having a multilayer system with layers 1-3 stacked one above another, said layers including a soft-magnetic layer 2, a hard- magnetic layer 1, and a tunnel oxide layer 3 disposed between said soft-magnetic layer and said hard-magnetic layer; word lines 4; bits lines 5 crossing said word lines at each of said magnetoresistive memory cells; a writing control circuit for impressing write currents in each case onto a respective word line and a respective bit line of a respective memory cell selected for writing, said writing control circuit having a write circuit for impressing the write currents in each case on said respective word line and said respective bit line causing the magnetic field produced by the superposition of the magnetic fields of the word line current and a bit line current to be precisely large enough to suffice for switching the magnetization of the soft magnetic layer in the selected memory cell but small enough that neither adjacent cells nor cells situated on the selected lines are switched see column 10, lines 32-52; Note: It is inherent that

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the term "adjacent" disclosed in column 10, lines 32-52 also refers to cells on the same selected line, said write circuit controlling the timings of the impression of both said word line current and said bit line current exactly causing the conventional switching of the soft magnetic layer of the selected memory cell to be transferred into a magnetization rotation with only the soft magnetic layer of the respective memory cell being rotated in a plurality of successive steps in a direction desired for writing a logic "0" or "1". Note: Application of word line current lwx and bit line current lwy are done in a specified time period of 1ns so that the magnetization direction is switched according to FIG. 9A-9E (see column 9, line 46 – column 10, line 12. Additionally, it is inherent to write either a logic "0" or logic "1" to a memory cell.

Allowable Subject Matter

7. Claims 2 and 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record considered pertinent to the applicant's disclosure, whether taken individually or in combination, does not teach or suggest: impressing the write currents for the selected memory cell in each case in approximately a same duration and in a manner offset in time with respect to one another by half of their switching duration (see claim 2), impressing a write bit line current in the same direction as a write word line current, and in a delayed manner

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when writing a logic "1" (see claim 5), the steps of rotating a magnetization direction as outlined in claim 7, lines 1-19.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kretelia Graham whose telephone number is (571) 272-5055. The examiner can normally be reached on Mon-Fri 8am-4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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